IN THE CLAIMS

1-12. (Cancelled)

13. (Original) An integrated circuit (IC) device comprising:

an elastic buffer having an input to receive a plurality of symbol sequences that were transmitted by another IC device over a serial point to point link, the elastic buffer to provide a plurality of buffered symbol sequences; and

deskew circuitry having an input coupled to an output of the elastic buffer, the deskew circuitry to forward the plurality of buffered symbol sequences with reduced skew in response to an enable control signal being asserted, the deskew circuitry includes

a plurality of deskew buffers,

write pointer logic to load the plurality of buffered symbol sequences into the plurality of deskew buffers,

read pointer logic to provide a plurality of read pointers to unload the plurality of buffered symbol sequences from the plurality of deskew buffers, and

control logic having an output coupled to the read pointer logic, the control logic to, in response to the first instance of a first, predetermined non-data symbol appearing at an output of one of the plurality of deskew buffers since the enable control signal was asserted, a) stall the read pointer for said deskew buffer, and b) generate an instance of a second, different predetermined non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said deskew buffer is forwarded.

14. (Original) The IC device of claim 13 wherein the read pointer is to be stalled at an entry that contains an instance of the first non-data symbol.

15. (Original) The IC device of claim 13 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

16. (Original) The IC device of claim 15 wherein the control logic is to, in response to detecting that a first instance of the first non-data symbol is followed by an instance of the

second non-data symbol that are to be loaded into one of the plurality of deskew buffers, a) stall the read pointer for another one of the plurality of deskew buffers after having loaded a second instance of the first non-data symbol that is clock aligned with the first instance, and b) generate an instance of the second non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said another deskew buffer is forwarded while preventing said instance of the second non-data symbol, that was detected, from being loaded into said one of the plurality of deskew buffers.

17. (Original) The IC device of claim 16 wherein the read pointer is to be stalled for said another deskew buffer at an entry that contains a data symbol.

18. (Original) The IC device of claim 13 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

19. (Original) A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial, point to point link, the circuitry includes

an elastic buffer having an input to receive a plurality of symbol sequences that were transmitted by another device over the serial point to point link, the elastic buffer to provide a plurality of buffered symbol sequences, and

deskew circuitry having an input coupled to an output of the elastic buffer, the deskew circuitry to forward the plurality of buffered symbol sequences with reduced skew in response to an enable control signal being asserted, the deskew logic includes

a plurality of deskew buffers,

write pointer logic to load the plurality of buffered symbol sequences into the plurality of deskew buffers,

read pointer logic to provide a plurality of read pointers to unload the plurality of buffered symbol sequences from the plurality of deskew buffers, and

control logic having an output coupled to the read pointer logic, the control logic to, in response to the first instance of a first, predetermined non-data symbol appearing at an output of one of the plurality of deskew buffers since the enable control signal was asserted, a) stall the read pointer for said deskew buffer, and b) generate an instance of a second, different predetermined non-data symbol at an output of the deskew circuitry through which the buffered symbol sequence for said deskew buffer is forwarded.

20. (Original) The system of claim 19 wherein the read pointer is to be stalled at an entry that contains an instance of the first non-data symbol.

21. (Original) The system of claim 20 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

22. (Original) The system of claim 19 wherein the control logic is to a) release the read pointer and b) stop generating instances of the second predetermined non-data symbol, if an instance of the first predetermined non-data symbol has appeared at an output of every one of the plurality of deskew buffers.

23. (Original) The system of claim 22 wherein the control logic is to, in response to an indication that a predetermined non-data symbol sequence is about to be loaded into one of the plurality of deskew buffers, stall the read pointer for another one of the plurality of deskew buffers and generate an instance of the second non-data symbol at an output of the deskew logic through which the buffered symbol sequence for said another deskew buffer is forwarded.

24. (Original) The system of claim 23 wherein the read pointer is to be stalled for said another deskew buffer an entry that contains a data symbol.

25. (Original) The system of claim 19 wherein the first non-data symbol is a PCI Express COM and the second non-data symbol is a PCI Express SKP.

26. (Original) The system of claim 19 further comprising a graphics element; and

wherein the IC device is a memory controller hub (MCH) that communicatively couples the processor to the main memory and the graphics element.

27. (Original) The system of claim 19 wherein the IC device is an I/O controller hub that communicatively couples the processor to peripheral devices.

28. (Original) The system of claim 23 wherein the predetermined non-data symbol sequence includes an instance of the first non-data symbol followed by an instance of the second non-data symbol, the instance of the first symbol but not the second symbol being loaded into said one of the plurality of deskew buffers.

29. (New) The IC device of claim 13 wherein the instance of the second, different predetermined non-data symbol is generated immediately preceding an instance of the first non-data symbol.

30. (New) The IC device of claim 13 wherein the instance of the second, different predetermined non-data symbol is inserted only at the output of the deskew circuitry.

31. (New) The system of claim 19 wherein the instance of the second, different predetermined non-data symbol is generated immediately preceding an instance of the first non-data symbol.

32. (New) The system of claim 19 wherein the instance of the second, different predetermined non-data symbol is inserted only at the output of the deskew circuitry.

33. (New) The IC device of claim 13 further comprising a plurality of IC devices having an input, wherein a plurality of instances of the second, different predetermined non-data symbol are inserted at an output of the deskew circuitry of at least one, but fewer than all of, the plurality of IC devices.

34. (New) The system of claim 19 further comprising a plurality of IC devices coupled to the processor, wherein a plurality of instances of the second, different predetermined non-data symbol are inserted at an output of the deskew circuitry of at least one, but fewer than all of, the plurality of IC devices.